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EXAMINER	
RASHID, DAVID	
ART UNIT	**PAPER NUMBER**
2624	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/708,515	GORDON ET AL.	
	Examiner	Art Unit	
	David P. Rashid	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/14/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-10, 12-16, 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

All of the examiner's suggestions presented herein below have been assumed for examination purposes, unless otherwise noted.

Amendments

1. This office action is responsive to the preliminary claim and specification amendment received on 9/14/2007. **Claims 1, 3 – 10, 12 – 16,** and **18 – 20** remain pending; **claims 2, 11,** and **17** are cancelled.

Drawings

2. The following is a quote from 37 CFR 1.84(p)(3):

> (3) Numbers, letters, and reference characters must measure at least.32 cm. (1 /8 inch) in height. They should not be placed in the drawing so as to interfere with its comprehension. Therefore, they should not cross or mingle with the lines. They should not be placed upon hatched or shaded surfaces. When necessary, such as indicating a surface or cross section, a reference character may be underlined and a blank space may be left in the hatching or shading where the character occurs so that it appears distinct.

3. FIG. 6 is objected to under 37 CFR 1.84(p)(3) as "microprocessor" element 144 cross/mingles with the right side line of the box.

4. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either

"Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. In response to applicant's specification amendments and remarks received on 9/14/2007, the previous specification objections are withdrawn.

Claim Objections

6. In response to applicant's claim objections amendments and remarks received on 9/14/2007, the previous claim objections are withdrawn.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 1, 3, 8 – 10, 12, 16,** and **18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Robles et al. (US 2004/0005089 A1) in view of Papadopoulou et al. (US 6,178,539 B1).

Regarding **claim 1**, while Robles discloses a method of creating a photomask layout (FIG. 5) for projecting an image of an integrated circuit design (paragraphs [0003], [0004]) comprising:

creating a layout (FIG. 3) of spaced (FIG. 3, element 315) integrated circuit shapes (FIG. 3, elements 310, 320) to be projected via the photomask;

creating bisectors ("centered between them" and "at some predetermined distances" in paragraph [0017] for the SRAF's to be placed) next to the spaced integrated circuit shapes;

determining bisectors ("centered between them" and "at some predetermined distances" in paragraph [0017]) between adjacent ones (FIG. 3) of the spaced integrated circuit shapes, the bisectors comprising locus of points equidistant from edges of the adjacent spaced integrated circuit shapes ("SRAF 335 centered between them", paragraph [0017] suggested that the bisector from which the SRAF has been placed is equidistant because it is "centered", as also supported in FIG. 3) and defining shared boundaries (the bisectors from which SRAF's are placed "define" shared boundaries, seeing an SRAF tells one of ordinary skill in the art that there is a shared boundary between the two edges); and

creating sub-resolution assist features (FIG. 3, elements 335, 355) along at least some of the bisectors between the adjacent ones of the spaced integrated circuit shapes, Robles does not teach

(i) creating Voronoi cells around the spaced integrated circuit shapes, and

(ii) the bisectors defining shared boundaries of the adjacent Voronoi cells.

Papadopoulou discloses determining critical area for circuit layouts using Voronoi diagrams (FIG. 22) that teaches

creating a layout of spaced integrated circuit shapes (polygons in FIG. 5);

creating Voronoi cells (FIG. 5) around the spaced integrated circuit shapes;

determining bisectors (the bold lines of FIG. 5; FIG. 4 arrow) between adjacent ones of the spaced integrated circuit shapes, the bisectors comprising locus of points equidistant (Col. 5, line 66 – Col. 6, line 2) from edges of the adjacent spaced integrated circuit shapes and defining shared boundaries (defining the shared boundary is the bold bisector line/arrow itself in FIG. 4, FIG. 5, and so forth) of adjacent Voronoi cells.

It would have been obvious to one of ordinary skill in the art at the time the invention was made (i) for the method of Robles to include creating Voronoi cells around the spaced integrated circuit shapes as taught by Papadopoulou and (ii) for the bisectors at predetermined distances of Robles to be the bisectors determined from the Voronoi cells as taught by Papadopoulou so that as "[t]he present disclosure further describes a method for speeding up the grid method of Wagner and Koren, in the above referenced article. The method is based on a low polynomial algorithm to compute critical area for shorts accurately in irregular rectilinear layouts.", Papadopoulou, Col. 5, lines 14 – 19 and that "[t]he method is presented for rectilinear layouts but it is extendible to general layouts.", Papadopoulou, Col. 5, lines 13 – 14.

Regarding **claim 3**, Robles discloses the method of claim 1 wherein the adjacent ones of the spaced integrated circuit shapes (FIG. 3, elements 310, 320 wherein the elements are "adjacent") are parallel to each other (elements 310 and 320 are also parallel to each other) and the sub-resolution assist features (FIG. 3, elements 335, 355) along the bisectors ("centered between them" and "predetermined distances" in paragraph [0017]) are parallel (FIG. 3, element 335 is parallel to elements 310 and 335) to the spaced integrated circuit shapes.

Regarding **claim 8**, Robles discloses the method of claim 1 wherein the integrated circuit shapes (FIG. 3, elements 310, 320) are two-dimensional (elements 310, 320 in FIG. 3 are two-dimensional) and include shapes having edges parallel (FIG. 3, elements 330/350 and 340 are parallel) and perpendicular (elements 310 and 320 in FIG. 3 contain edges other than edges 330/350 and 340 that are perpendicular) to each other, between which the bisectors are located (FIG. 3, elements 335, 355).

Regarding **claim 9**, Robles discloses the method of claim 1 wherein the integrated circuit shapes (FIG. 3, elements 310, 320) are two-dimensional (elements 310, 320 in FIG. 3 are two-dimensional) and include shapes having lengths of parallel edges (FIG. 3, elements 330 and 340 are parallel) in which an edge of one shape ends at a point (the bottom point of edge 340 in FIG. 3) within the length of the other shape (FIG. 3, element 330 continues to extend beyond the bottom point of edge 340 unto edge 350), between which the bisectors are located (FIG. 3, elements 335, 355).

Regarding **claim 10**, claim 1 recites identical features as in the program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps (FIG. 11, FIG. 12) as in claim 1. Thus, references/arguments equivalent to those presented above for claim 1 are equally applicable to claim 10.

Regarding **claim 12**, claim 3 recites identical features as in claim 12. Thus, references/arguments equivalent to those presented above for claim 3 are equally applicable to claim 12.

Regarding **claim 16**, claim 1 recites identical features as in the article manufacture comprising a computer-usable medium having computer readable program codes means

embodied therein (FIG. 11, FIG. 12) as in claim 1. Thus, references/arguments equivalent to those presented above for claim 1 are equally applicable to claim 10. All means-plus-function language is anticipated by Robles (FIG. 11, FIG. 12).

Regarding **claim 18**, claim 3 recites identical features as in claim 18. Thus, references/arguments equivalent to those presented above for claim 3 are equally applicable to claim 18.

9. **Claims 4, 13,** and **19** are rejected under 35 U.S.C. 103(a) as being unpatentable over the Robles et al. (US 2004/0005089 A1) in view of Papadopoulou et al. (US 6,178,539 B1) and LaCour (US 2002/0155357 A1).

Regarding **claim 4**, while Robles in view of Papadopoulou discloses the method of claim 1, Robles in view of Papadopoulou does not teach identifying different types of vertices for the bisectors prior to creating the sub-resolution assist features, and prioritizing creation of the sub-resolution assist features in accordance with the type of vertex.

LaCour discloses a prioritization application of resolution enhancement techniques (FIG. 6) that teaches identifying different types of vertices ("bars overlap to form a "+" structure" in paragraph [0057]; FIG. 6, element 610; paragraphs [0047] through [0052] where the vertices are either the "generating edges" and "facing edges" that may either be orthogonal or angled) for the bisectors (the bisectors being the lines from which the scattering bars of LaCour are being placed) prior to creating the sub-resolution assist features (the LaCour vertex listing in Col. 8, paragraphs [0047] through [0052] and [0057] has been already been created before the LaCour algorithm is implemented), and prioritizing creation ("the ends of both scattering bars can be

shortened to provide a "L" structure" in paragraph [0057]; FIG. 6, element 612; paragraphs [0053] through [0056]) of the sub-resolution assist features in accordance with the type of vertex.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to identify different types of vertices for the bisectors prior to creating the sub-resolution assist features, and prioritize creation of the sub-resolution assist features in accordance with the type of vertex as taught by LaCour "to improve lithography tools to improve the fidelity of the lithography process.", LaCour, paragraph [0022].

Regarding **claim 13**, claim 4 recites identical features as in claim 13. Thus, references/arguments equivalent to those presented above for claim 4 are equally applicable to claim 13.

Regarding **claim 19**, claim 4 recites identical features as in claim 19. Thus, references/arguments equivalent to those presented above for claim 4 are equally applicable to claim 19. All means-plus-function language is anticipated by Robles (FIG. 11, FIG. 12).

10. **Claims 5 – 6, 14 – 15,** and **20** are rejected under 35 U.S.C. 103(a) as being unpatentable over the Robles et al. (US 2004/0005089 A1) in view of Papadopoulou et al. (US 6,178,539 B1) and Lucas et al. (US 2004/0248016 A1).

Regarding **claims 5** and **6**, while Robles in view of Papadopoulou discloses the method of claim 1, Robles in view of Papadopoulou does not teach extending at least some of the sub-resolution assist features beyond the bisectors on which they are created to connect to other sub-resolution assist features.

Lucas discloses a method of designing a reticle and forming a semiconductor device therewith (paragraph [0006]) that extends (paragraph [0016]) at least some of the sub-resolution assist features (FIG. 3, element 56; FIG. 9, element 156) beyond the bisectors on which they are created to connect (FIG. 9, element 154) to other sub-resolution assist features (FIG. 3, element 52; FIG. 9, element 152).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to extend at least some of the sub-resolution assist features beyond the bisectors on which they are created to connect to other sub-resolution assist features as taught by Lucas "...for improved coverage of the assist features with improved process margin and reduced reticle inspection issues.", Lucas, paragraph [0023].

Regarding **claim 14**, claim 5 recites identical features as in claim 14. Thus, references/arguments equivalent to those presented above for claim 5 are equally applicable to claim 14.

Regarding **claim 15**, claim 6 recites identical features as in claim 15. Thus, references/arguments equivalent to those presented above for claim 6 are equally applicable to claim 15.

Regarding **claim 20**, claim 5 recites identical features as in claim 20. Thus, references/arguments equivalent to those presented above for claim 5 are equally applicable to claim 20.

11. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over the Robles et al. (US 2004/0005089 A1) in view of Papadopoulou et al. (US 6,178,539 B1) and Frankowsky (US 2002/0182523 A1).

Regarding **claim 7**, while Robles in view of Papadopoulou discloses the method of claim 1, Robles in view of Papadopoulou does not teach removing at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout.

Frankowsky discloses a method for carrying out a rule-based optical proximity correction with simultaneous scatter bar insertion (paragraph [0015]) that removes at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout (paragraph [0089]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to remove at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout as taught by Frankowsky because "[i]f these scatter bars were not removed, they would be imaged on the substrate in the exposure process in certain circumstances, which is undesirable.", Frankowsky, paragraph [0089].

Response to Arguments

12. Applicant's arguments filed on 9/14/2007 with respect to **claims 1, 3 – 10, 12 – 16,** and **18 – 20** have been respectfully and fully considered, they are not found persuasive.

13. **Summary of Remarks** regarding **claims 1, 10** and **16**:

(i) Applicant argues Roble makes no mention of any bisector that extends beyond the edge of his feature edge 340, to end in a 1D fragmented vertex (@ *response page 11*).

(ii) Roble does not disclose or suggest applicants' method as described in claims 1, 10, and 16. The Papadopoulou patent, cited against claims 2, 11, and 17 does not remedy the deficiencies of Roble. Papadopoulou does not use any boundaries of Voronoi cells to create subresolution assist features, let alone define shared boundaries of adjacent Voronoi cells as in applicants' claimed invention. Accordingly, one of ordinary skill in the art would not even look to combine the Roble and Papadopoulou references in the first instance (@ *response page 12*).

Even if the references were combined, there is no suggestion in either Roble or Papadopoulou to create a bisector that comprises the locus of points equidistant from edges of the adjacent spaced integrated circuit shapes and defines shared boundaries of adjacent Voronoi cells. Roble does not disclose or suggest a "bisector" that extends beyond the end of a feature edge that ends within the length of a parallel feature edge, as applicants' invention would need to do to create a bisector under similar conditions. Papadopoulou does not disclose or suggest creating bisectors along shared boundaries of adjacent Voronoi cells. As such, one skilled in this art would not arrive at applicants' claimed invention from the hypothetical combination of these references. Applicants submit that the rejection is based on hindsight only after reading applicants' only specification (@ *response pages 12 – 13*).

14. **Examiner's Response** regarding **claims 1, 10** and **16**:

(i) Though Robles makes no mention of any bisector that extends beyond the edge of his feature edge 340, to end in a 1D fragmented vertex, the claims in question cite creating SRAFs along "at least some of the bisectors" and Robles does in fact support where any parallel partition

between two edges creates a bisector and thus SRAF. The placing of the SRAFs along bisectors where two edges are parallel (FIG. 3, Robles) would be enough and no requirement for bisector extension is needed to anticipate the claims.

(ii) However, Papadopoulou does in fact remedy the deficiencies of Robles. Robles mentions placing the SRAFs between the edges "at some predetermined distances" and "center[ing] between them" (paragraph [0017], Robles) suggesting that any "distance algorithm" would suffice in determining bisector and SRAF placement, so long as it meets placing those elements between the edges "at some predetermined distances" and "center[ing] between them".

Papadopoulou is a method that creates Voronoi cells around spaced integrated circuit shapes (FIG. 5; FIG. 11, Papadopoulou), which includes determining bisectors (the bold lines of FIG. 5; FIG. 4 arrow, Papadopoulou) between adjacent ones of the spaced integrated circuit shapes, the bisectors comprising locus of points equidistant (Col. 5, line 66 – Col. 6, line 2, Papadopoulou) from edges of the adjacent spaced integrated circuit shapes and defining shared boundaries (defining the shared boundary is the bold bisector line/arrow itself in FIG. 4, FIG. 5, and so forth, Papadopoulou) of adjacent Voronoi cells.

FIG. 11 of Papadopoulou (though FIG. 5 is equally applicable) provides fairly straightforward reasoning why it would have been obvious to one of ordinary skill in the art at the time the invention was made for the bisector and SRAF placement of Robles to use Voronoi cells and bisectors from the Voronoi algorithm of Papadopoulou. Robles in determining its bisector and SRAF placement could use the Voronoi algorithm of Papadopoulou to achieve the same results for any parallel partition between two edges as evident in FIG. 11 of Papadopoulou and FIG. 3 of Robles.

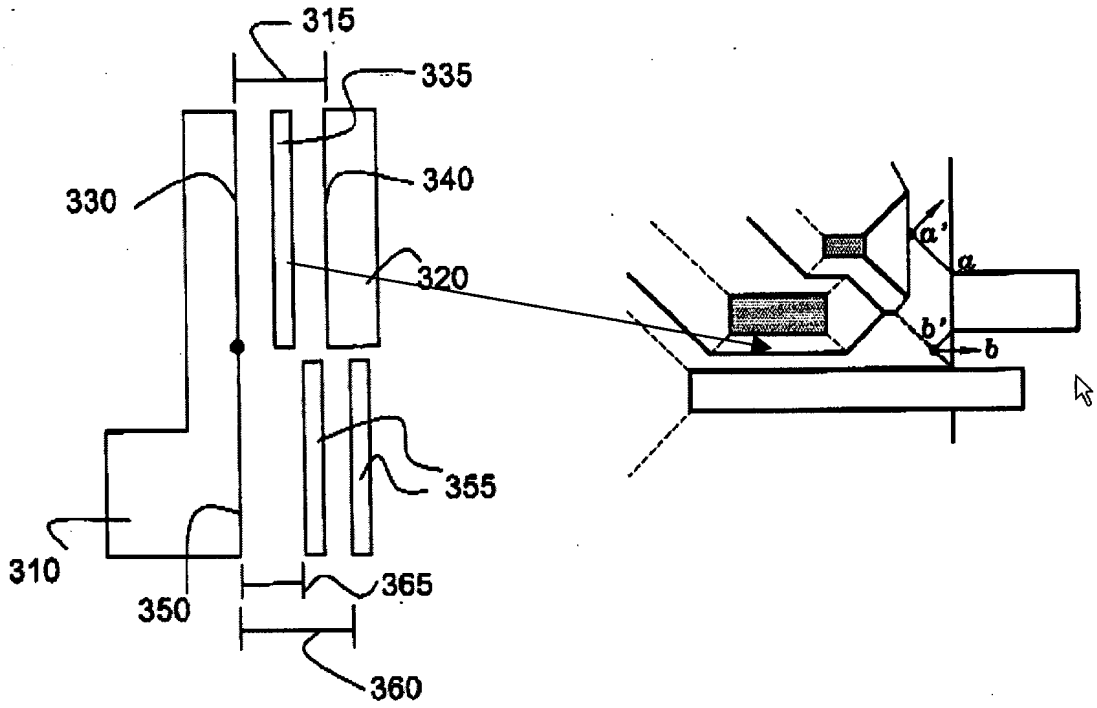

FIG. II

It would have been obvious to one of ordinary skill in the art at the time the invention was made (i) for the method of Robles to include creating Voronoi cells around the spaced integrated circuit shapes as taught by Papadopoulou and (ii) for the bisectors at predetermined distances of Robles to be the bisectors determined from the Voronoi cells as taught by Papadopoulou so that as "[t]he present disclosure further describes a method for speeding up the grid method of Wagner and Koren, in the above referenced article. The method is based on a low polynomial algorithm to compute critical area for shorts accurately in irregular rectilinear layouts.", Papadopoulou, Col. 5, lines 14 – 19 and that "[t]he method is presented for rectilinear layouts but it is extendible to general layouts.", Papadopoulou, Col. 5, lines 13 – 14.

In such an instance of two parallel edges in Robles, the Voronoi algorithm of Papadopoulou would create the same bisectors for SRAF foundation of Robles, as it is only required that SRAFs are along "at least some of the bisectors between the adjacent ones", and the

anticipation of Robles in view of Papadopoulou is whole (without the requirement that the bisector extends beyond the end of a feature edge that ends within the length of a parallel feature edge).

15. **Summary of Remarks** regarding **claims 4, 13** and **19**:

Applicant argues that since the definition of "bisector" has been modified in independent claims 1, 10, and 16, such definition caries to describe the "vertices for the bisectors" as recited in the dependent claims in question. The classification of LaCour has nothing to do with the type of vertices of bisectors, as applicants have defined (*@ response page 13*).

16. **Examiner's Response** regarding **claims 4, 13** and **19**:

Robles in view of Papadopoulou uses the Voronoi algorithm to create "vertices for the bisectors" (all vertices as shown in FIG. 5 or FIG. 11, Papadopoulou). LaCour does in fact describe classification with the type of vertices of bisectors (e.g. a "+" shaped vertex is changed to "L" shaped as described in the rejection above). It would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to identify different types of vertices for the bisectors prior to creating the sub-resolution assist features, and prioritize creation of the sub-resolution assist features in accordance with the type of vertex as taught by LaCour "to improve lithography tools to improve the fidelity of the lithography process.", LaCour, paragraph [0022].

17. **Summary of Remarks** regarding **claims 5, 6, 14, 15,** and **20**:

Applicant argues that Lucas makes no mention of extending SRAF beyond bisectors as defined by applicants. Lucas does not disclose or suggest the extension of SRAF along bisectors defined by shared boundaries of adjacent Voronoi cells. Lucas merely links SRAF in a manner unrelated to applicants' claimed method (@ *response page 14*).

18. **Examiner's Response** regarding **claims 5, 6, 14, 15,** and **20**:

A Varanoi bisector of Robles in view of Papadopoulou would eventually stop before coming into "contact" with a circuit feature edge, as supported in FIG. 3, element 56 of Lucas. FIG. 9, element 162 of Lucas extends the SRAF outside the limitations of the Varanoi bisector of Robles in view of Papadopoulou. It would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to extend at least some of the sub-resolution assist features beyond the bisectors on which they are created to connect to other sub-resolution assist features as taught by Lucas "...for improved coverage of the assist features with improved process margin and reduced reticle inspection issues.", Lucas, paragraph [0023].

19. **Summary of Remarks** regarding **claim 7:**

Applicant argues that Frankowsky merely removes scatter bars in a manner unrelated to applicants' claimed method and does not disclose or suggest the removal of SRAF along bisectors defined by shared boundaries of adjacent Varonoi cells. Therefore, there is no disclosure of applicants' claimed method in the combination of Roble and Frankowsky (@ *response page 14*).

20. **Examiner's Response** regarding **claim 7:**

Just because Frankowsky removes scatter bars in a manner unrelated to applicants' claimed method does not prohibit its anticipation to the claim in question that requires "removing at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout". Frankowsky gives a clear motivation of why it would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to remove at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout as taught by Frankowsky because "[i]f these scatter bars were not removed, they would be imaged on the substrate in the exposure process in certain circumstances, which is undesirable.", Frankowsky, paragraph [0089].

Conclusion

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David P. Rashid whose telephone number is (571) 270-1578. The examiner can normally be reached Monday - Friday 8:30 - 17:00 ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Werner can be reached on (571) 272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David P. Rashid/
Examiner, Art Unit 2624

David P Rashid
Examiner
Art Unit 2624

VIKRAM BALI
PRIMARY EXAMINER